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CYPRESS/BLAKELY
BLAKELY SOKOLOFF TAYLOR & ZAFMAN
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

EXAMINER	
LAI, ANDREW	

ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/777,286	GUPTA ET AL.	
	Examiner	Art Unit	
	ANDREW LAI	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 9-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 9-28* is/are rejected.

7)☒ Claim(s) *7 and 29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/14/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3, 5-6, 11-13, 16-16, 20 and 23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Minoda (US 5,731,770) in view of Burk et al (US 2003/0169626, Burk hereinafter) and further in view of Costello (US 4,777,485).

Minoda discloses "a digital data buffering device" (col. 1 lines 4-5, and see fig. 6, which depicts "a block diagram showing the schematic structure" thereof, as recited col. 3 lines 33-34) having (see fig. 6) "An input rate calculator 205 (average rate calculating means), the clock generator 206 (transfer rate controlling means), and a read address generator 204 (second address generating means)" (col. 6 lines 44-47) and further comprising the following features:

- **With respect to Independent claims 1, 15, 20, 23 and 28**

Regarding claims 1 and 28, *a method* ("correction method", col. 8 line 4), *comprising*

calculating a variation between an input data rate and a predetermined output data rate (refer to fig. 6 and see "with the structure of the input rate calculator 205, the average of input rates of data after the conversion of the sampling rate in a given period of time, and the difference between the average input rate and a reference

output rate are calculated", col. 7 lines 20-24), *the input data rate being based on a number of data read requests* (see "count n represents a value corresponding to the average input rate in a given period… The reference value N indicates a value corresponding to the reference output rate.", col. 7 lines 33-34, which n is a result of counting the data read into the buffer as the follows, in reference to fig. 9 showing internal structure of input rate calculator 205, "the pulse signal a_1 is input to the counter 501 from the write address generator 202. The counter 501 counts the number of pulses of the pulse signal a_1, and inputs the count n to the latch section 502 … the latch section 502 latches the count n counted just before the reset and inputs the count n to the comparator 504", col. 7 lines 25-32), *wherein calculating the variation* (the "difference" cited above) *comprises updating a counter value representative of the variation* ("the difference is input to the controlling section", col. 3 lines 2-3, which, as obvious to one skilled in the art, keeps *a counter value* updated as *representative of the variation*); *and*

compensating for the variation (refer to fig. 7 and see "correcting the difference between the average input rate and the reference output rate according to the content of the correction rate table 301", col. 8 lines 14-16, and further "matches the difference between the average input rate and the reference output rate", col. 8 lines 22-23) *by modifying the number of data read requests* (see "The read address generator 204 is a circuit for generating the address of output data according to clocks generated by the clock generator 206", col. 6 lines 50-52 and further "the clock generator 206 is provided with a correction rate table 301. The correction rate table 301 stores a correction method as a table, for correcting the difference

between the average input rate … and the reference output rate", col. 8 lines 2-6, which then effectively *modifies the number of data read requests* because the clock generator, as disclosed, will provide the corrected clocks to read address generator 204, which in turn generates the address for reading output data per the corrected clocks), *and wherein compensating for the variation comprises …*

Regarding claim 15, *an apparatus* ("digital data buffering device", col. 1 lines 4-5 and fig. 6), *comprising:*

an encapsulator engine (fig. 6 "read address generator 204"); *and*

a packet pre-processor (fig. 6 "input rate calculator 205", "address selection/read and write timing generator 203" and "clock generator 206") *coupled to the encapsulator engine* (fig. 6 depicting such coupling), *the packet pre-processor to calculate a variation between an input data rate and a pre-determined output data rate* (fig. 6 and see "with the structure of the input rate calculator 205, the average of input rates of data after the conversion of the sampling rate in a given period of time, and the difference between the average input rate and a reference output rate are calculated", col. 7 lines 20-24) *and to update a counter value representative of the variation* ("the difference is input to the controlling section", col. 3 lines 2-3, which, as obvious to one skilled in the art, keeps *a counter value* updated as *representative of the variation*), *the input data rate being based on a number of data read requests* (see "count n represents a value corresponding to the average input rate in a given period… The reference value N indicates a value corresponding to the reference output rate.", col. 7 lines 33-34, which n is a result of counting the data read in as the follows, in reference to fig. 9 showing internal structure of input rate calculator 205,

"the pulse signal a_1 is input to the counter 501 from the write address generator 202. The counter 501 counts the number of pulses of the pulse signal a_1, and inputs the count n to the latch section 502 … the latch section 502 latches the count n counted just before the reset and inputs the count n to the comparator 504", col. 7 lines 25-32), *the packet pre-processor to compensate for the variation* (refer to fig. 7 and see "the clock generator 206 is provided with a correction table 301. The correction rate table 301 stores a correction method as a table, for correcting the difference between the average input rate and the reference output rate according to the content of the correction rate table 301", col. 8 lines 14-16, and further "matches the difference between the average input rate and the reference output rate", col. 8 lines 22-23) *by modifying the number of data read requests* (see "The read address generator 204 is a circuit for generating the address of output data according to clocks generated by the clock generator 206", col. 6 lines 50-52 and further "the clock generator 206 is provided with a correction rate table 301. The correction rate table 301 stores a correction method as a table, for correcting the difference between the average input rate … and the reference output rate", col. 8 lines 2-6, which then effectively *modifies the number of data read requests* because the clock generator, as disclosed, will provide the corrected clocks to read address generator 204, which in turn generates the address for reading output data per the corrected clocks), *wherein the packet pre-processor* ("input rate calculator 205") *is configured to compensate for the variation by…*

Regarding claim 20, *an apparatus* (see "a digital data buffering device", col. 1 lines 4-5, and fig. 6, which depicting such), *comprising:*

means for transmitting data through a communication channel (fig. 6 “parallel/serial converter 207”, which “outputs data … to be input to a D/A converter", col. 6 lines 29-31) *having a bandwidth* (see “The reference value N indicates a value of corresponding to the reference output rate”, col. 7 lines 35-36, noting that an output rate “N” necessarily indicates/requires matching *bandwidth*);

means for calculating a variation between an input data rate and a pre-determined output data rate (refer to fig. 6 and see “with the structure of the input rate calculator 205, the average of input rates of data after the conversion of the sampling rate in a given period of time, and the difference between the average input rate and a reference output rate are calculated", col. 7 lines 20-24)*, the input data rate being based on a number of data read requests* (see “count n represents a value corresponding to the average input rate in a given period… The reference value N indicates a value corresponding to the reference output rate.”, col. 7 lines 33-34, which n is a result of counting the data read into the buffer as the follows, in reference to fig. 9 showing internal structure of input rate calculator 205, "the pulse signal a_1 is input to the counter 501 from the write address generator 202. The counter 501 counts the number of pulses of the pulse signal a_1, and inputs the count n to the latch section 502 … the latch section 502 latches the count n counted just before the reset and inputs the count n to the comparator 504", col. 7 lines 25-32);

means for compensating for the variation (refer to fig. 7 and see “correcting the difference between the average input rate and the reference output rate according to the content of the correction rate table 301”, col. 8 lines 14-16, and further “matches the difference between the average input rate and the reference

output rate", col. 8 lines 22-23) *to increase a utilization efficiency of the bandwidth* ("to provide a digital data buffering device capable of preventing deterioration of the quality of output signals of digital data", col. 2 lines 7-8, and also "a fluctuation of the transfer rate of the output data is prevented", Abstract lines 11-14, effectively *increasing utilization efficiency of the bandwidth*), *wherein the means for compensating for the variation comprises…*

Regarding claim 23, *a system* (fig. 1, "a sampling rate converter", col. 3 line 17), *comprising:*

a link layer device (fig. 1 the portion between "input interface 2" and "output interface 8", which portion, "link portion" hereinafter, links the "input interface 2" and the "output interface 8" as shown in fig. 1);

a first physical interface device (fig. 1 "input interface 2"); *and*

a framer (fig. 6, a "digital data buffering device", col. 3 line 34, which "is applied to the output interface 8 [of fig. 1]", col. 6 line 24) *coupled to the link layer device* (said "link portion" of fig. 1) *and the first physical interface device* (said "input interface 2" of fig. 1), *wherein the framer comprises an encapsulator engine* (fig. 6 "parallel/serial converter 207") *and a packet pre-processor* (fig. 6 items 201-206, "pre-processor" hereinafter, comprising, e.g., "write address generator 202", "input rate calculator 205, "clock generator 206", "read address generator 204", etc.) *coupled to the encapsulator engine* (fig. 6 depicting the coupling between the "pre-processor" and "parallel/serial converter 207"), *the packet pre-processor to calculate a variation between an input data rate and a pre-determined output data rate* (see "with the structure of the input rate calculator 205, the average of input rates of data

after the conversion of the sampling rate in a given period of time, and the difference between the average input rate and a reference output rate are calculated", col. 7 lines 20-24) *and to update a counter value representative of the variation* ("the difference is input to the controlling section", col. 3 lines 2-3, which, as obvious to one skilled in the art, keeps *a counter value* updated as *representative of the variation*), *the input data rate being based on a number of data read requests* (see "count n represents a value corresponding to the average input rate in a given period… The reference value N indicates a value corresponding to the reference output rate.", col. 7 lines 33-34, which n is a result of counting the data read into the buffer as the follows, in reference to fig. 9 showing internal structure of input rate calculator 205, "the pulse signal a_1 is input to the counter 501 from the write address generator 202. The counter 501 counts the number of pulses of the pulse signal a_1, and inputs the count n to the latch section 502 … the latch section 502 latches the count n counted just before the reset and inputs the count n to the comparator 504", col. 7 lines 25-32), *the packet pre-processor to compensate for the variation* (refer to fig. 7 and see "the clock generator 206 is provided with a correction rate table 301. The correction rate table 301 stores a correction method as a table, for correcting the difference between the average input rate and the reference output rate according to the content of the correction rate table 301", col. 8 lines 14-16, and further "The speed correction amount calculator 303 matches the difference between the average input rate and the reference output rate", col. 8 lines 22-23) *by modifying the number of data read requests* (see "The read address generator 204 is a circuit for generating the address of output data according to clocks generated

by the clock generator 206", col. 6 lines 50-52, which then effectively *modifies the number of data read requests* because the clock generator, as disclosed, will provide the corrected clocks to read address generator 204, which in turn generates the address for reading output data per the corrected clocks), *wherein the packet pre-processor* (fig. 6 items 201-206) *is configured to compensate for the variation* ("the difference") *by*…

Regarding claims 1, 15 and 23, matching difference between *data read request* ("n") and output rate ("N") ("The speed correction amount calculator 303 matches the difference between the average input rate [n] and the reference output rate [N]", col. 8 lines 22-24) *when the counter value is either equal to or less than a lower threshold value* (see, e.g., "When the relation between the count n and the reference value N is n > ($1.02\times N$), the count n is judged to be (+2%), i.e., 2% ahead of the reference value N", col. 7 lines 54-56, indicating *a lower threshold* "$-0.02N$" because in this $n > 1.02N$ case the *variation* $\Delta = (N - n) < (N - 1.02N) = -0.02N$, or simply $\Delta < -0.02N$, i.e., *the counter value* (Δ) *is either equal to or less than* ($<$) *a lower threshold value* ($-0.02N$). For later convenience of discussion, this is denoted as "**A**head-of case" or simply "**A** case"); *and*

when the counter value is either equal to or greater than an upper threshold value (see, e.g., "When the relation between the count n and the reference value N is n < ($0.98\times N$), the count n is judged to be (-2%), i.e., 2% behind the reference value N", col. 7 lines 41-43, indicating *an upper threshold* "$+0.02N$" because in this $n < 0.98N$ case the *variation* $\Delta = (N - n) > (N - 0.98N) = +0.02N$, or simply $\Delta > +0.02N$, i.e., *the counter value* (Δ) *is either equal to or greater than* ($>$) *an upper threshold value*

(+0.02N). For later convenience of discussion, this is denoted as "**B**ehind case" or simply "**B** case").

Regarding claim 20, *means for* matching difference between *data read request* ("n") and output rate ("N") ("The speed correction amount calculator 303 matches the difference between the average input rate [n] and the reference output rate [N]", col. 8 lines 22-24) *when the variation exceeds a first threshold value of* (see, e.g., "When the relation between the count n and the reference value N is n > (1.02×N), the count n is judged to be (+2%), i.e., 2% ahead of the reference value N", col. 7 lines 54-56, resulting in an above cited "**A** case") *of a pre-determined range* (this "**A** case" together with the "**B** case" below gives a *pre-determined range* of "±0.02N" in absolute terms or "±2%" in relative terms for the *variation* Δ, see further discussion below. In addition, Minoda discloses "it is also possible to judge the difference [*variation*] by ±P % (P is an arbitrary value)", col. 7 lines 64-65), *and*

when the variation exceeds a second threshold value (see, e.g., "When the relation between the count n and the reference value N is n < (0.98×N), the count n is judged to be (-2%), i.e., 2% behind the reference value N", col. 7 lines 41-43, resulting in an above cited "**A** case") *of a pre-determined range* (this "**B** case" together with the "**A** case" above gives a *pre-determined range* of "±0.02N", as already discussed above).

Regarding claim 28, matching difference between *data read request* ("n") and output rate ("N") ("The speed correction amount calculator 303 matches the difference between the average input rate [n] and the reference output rate [N]", col. 8 lines 22-24) *when the counter value is either equal to or greater than an upper*

threshold value (see, e.g., "When the relation between the count n and the reference value N is $n > (1.02 \times N)$, the count n is judged to be (+2%), i.e., 2% ahead of the reference value N", col. 7 lines 54-56, indicating *an upper threshold* "$+0.02N$" because in this $n > 1.02N$ case the *variation* $\Delta = (n - N) > (1.02N - N) = 0.02N$, or simply $\Delta > +0.02N$, i.e., *the counter value* (Δ) *is either equal to or greater than* (>) *an upper threshold value* ($+0.02N$). This is an above cited "**A** case".); *and*

when the counter value is either equal to or less than a lower threshold value (see, e.g., "When the relation between the count n and the reference value N is $n < (0.98 \times N)$, the count n is judged to be (−2%), i.e., 2% behind the reference value N", col. 7 lines 41-43, indicating *a lower threshold* "$-0.02N$" because in this $n < 0.98N$ case the *variation* $\Delta = (n - N) < (0.98N - N) = -0.02N$, or simply $\Delta < -0.02N$, i.e., i.e., *the counter value* (Δ) *is either equal to or less than* (<) *a lower threshold value* ($-0.02N$). This is an above cited "**B** case").

(**Examiner's note**: It is noted herein that claims 28 and 1 are essentially the same. The only difference is that the so-called *variation* or *counter value* in claim 1 is "output rate − input rate" while in claim 28 it is the opposite, i.e., "input rate − output rate". Defining the *variation* or *counter value* in either way has no advantage or disadvantage over the other.)

To sum up, Minoda discloses matching the difference between *read request* and output data rate for both "**A** case" and "**B** case" without expressly teaching how differently the "matching" is done. However, it is clear to one skilled in the art that there are essentially two options for either case. For "**A** case" wherein *read requests* would be ahead of or faster than output rate, one would either slow down input reading (*masking read request*, "Action **In**" hereinafter to indicate action taken at the **In**put side) or speed up output in order to avoid output bandwidth congestion ("Action **Out**" hereinafter indicating action taken at the **Out**put side). For "**B** case"

wherein *read requests* would be behind or slower than output rate, one would either speed up input reading (*generating additional read requests*, "Action **In**") or speed up output in order to meet desired outgoing transmission ("Action **Out**").

Minoda does not expressly teach which one of the two options to use.

Burk discloses "system and method for controlling a number of outstanding data transactions" (Title) "within an integrated circuit used in a graphics system" ([0002] lines 3-4) having an "interface controller" (fig. 9) comprising a "read issuer" (fig. 9 item 252) for controlling "read requests" from other components. Burk's invention comprises:

Regarding claims 1, 15, 20, 23 and 28, *masking a data read request when* in the "**A** case" ("the read issuer 252 is configured to receive read requests and selectively issue of inhibit those read transactions initiated by those requests", [0086] lines 1-3, and "the read issuer 252 may temporarily inhibit performance of the read transaction initiated by the read request (e.g., by buffering the read request and delaying to provide the read request to an interface 222)", page 7 left col. lines 5-6, "until the risk of congestion and/or deadlock has decreased to an acceptable level", page 7 left col. lines 13-15).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system/method of Minoda by adding the expressly taught method by Burk of inhibiting or *masking read requests* ("Action **In**" cited above, noting again that Minoda's "rate matching" can only choose either "Action **In** " or "Action **out**") for minimizing "risk of congestion" in order to provide a more controlled process to overcome prior art deficiencies wherein "because each external read may

initiate several internal data transactions, an integrated circuit's performance may be reduced if too many reads are initiated" (Burk, page 2 left col. lines 7-9).

It is noted that Burk also indirectly or implicitly provided teachings, in the "**B** case", of *generating additional data read requests* (see "determining whether too many read transactions are currently outstanding may involve adding a number of data transactions that will be initiated by the read request received at 802 to a number of currently outstanding data transactions", [0094] lines 1-5).

However, Minoda in view of Burk does not expressly disclose said feature.

Costello discloses "method and apparatus for DMA [direct memory access] window display" (Title) which has "particular application for use in displaying digital images in an animated form on a CRT display" (Abstract lines 2-4) comprising:

generating additional read requests in the "**B** case" (see, in view of fig. 1, "in the event additional frames are to be displayed to provide an animated effect, DMA controller 20 sets a new base address for the next memory access and initiates additional read operations", col. 5 lines 57-60).

It would have been obvious to one of ordinary skill in the art at the time of the invention to further modify the method/system of Minoda by adding the expressly taught method by Costello of initiating or *generating additional read requests* ("Action **In**" cited above, noting that Minoda's "rate matching" can only take either "Action **In**" or "Action **Out**") in order to provide a smoother moving image display mechanism that "permits images stored in memory to be displayed within a window on a CRT at a rate which permits an animation effect to be achieved" (Costello, col. 2 lines 2-4), "such as in a television or movie presentation" (Costello, col. 1 line 60).

- **With respect to Dependent claims**

Minoda discloses the following features:

Regarding claim 2, *wherein the variation is compensated to increase a bandwidth in a communication channel* (see, e.g. "When the relation between the count n and the reference value N is $n < (0.98 \times N)$, the count n is judged to be (-2%), i.e., 2% behind the reference value N", col. 7 lines 41-43, and then "The speed correction amount calculator 303 matches the difference between the average input rate [n] and the reference output rate [N]", col. 8 lines 22-24, noting that said "matches the difference" in this case speeds up "input rate", effectively *increases a bandwidth*).

Regarding claim 3, *wherein the variation is compensated to increase the bandwidth* (see discussion above for claim 2, *increasing bandwidth in a communication channel*, which applies hereto) *in a plurality of communication channels* (see fig. 6 depicting "parallel/serial converter 207" which suggests *a plurality of communication channels*).

Regarding claim 5, *wherein modifying the number of data read requests comprises* rate matching *for a plurality of data read requests* (for above cited "**B**ehind case", see, e.g. "When the relation between the count n and the reference value N is $n < (0.98 \times N)$, the count n is judged to be (-2%), i.e., 2% behind the reference value N", col. 7 lines 41-43, and then "The speed correction amount calculator 303 matches the difference between the average input rate [n] and the reference output rate [N]", col. 8 lines 22-24. And it is done for *plurality of read requests* depending on the needs; see for example col. 7 lines 44-46 for the case of

"1% behind the reference value N", and in general "−p%" behind wherein "p is an arbitrary number", col. 7 lines 64-65).

Regarding claim 6, *wherein modifying the number of data read requests comprises* rate matching for *a plurality of data read requests* (for above cited "**A**head of case", see, e.g. "When the relation between the count n and the reference value N is n > (1.02×N), the count n is judged to be (+2%), i.e., 2% ahead of the reference value N", col. 7 lines 54-56, and then "The speed correction amount calculator 303 matches the difference between the average input rate [n] and the reference output rate [N]", col. 8 lines 22-24. And it is done for *plurality of read requests* depending on the needs; see for example col. 7 lines 51-53 for the case of "1% ahead of the reference value N", and in general "+p%" ahead of wherein "p is an arbitrary number", col. 7 lines 64-65).

Regarding claim 11, *comparing a total bit group of data received* ("count n" cited above) *by a packet encapsulator* ("digital data buffering device" cited above) *from a data read request with a counter value* ("reference value N" cited above) (see fig. 9 "comparator 504" taking said "count n" and "reference value (N)" as inputs for *comparing*);

Regarding claim 12, *wherein the total bit group of data is a byte* (it is notorious old and well known in the art that digital data formed with information in bits and *bytes* wherein each *byte* has eight bits).

Regarding claim 16, *a pre-compute circuitry* (fig. 7 "counter 501" and "latch section 502") *to calculate a total bit group of data received* ("count n" cited above and shown in fig. 7 as output from said "latch section 502", for which see "The latch

section 502 latches the count n counted by the counter 501", col. 7 lines 5-6) *by the packet pre-processor at the input data rate* (see "The count n represents a value corresponding to the average input rate in a given period", col. 7 lines 33-34); *and*

a request modifier circuitry (fig. 7, "comparator 504" and "clock generator 206") *coupled to the pre-compute circuitry* (fig. 7 depicting such coupling), *the request modifier circuitry to determine a difference between the total big group of data calculated by the pre-compute circuitry* (fig. 7 depicting "count n" as an input to said "comparator 504") *and a predetermined output data bus width* (fig. 7 "reference value (N)", and see further "The comparator 504 compares the count n latched by the latch section 502 and the reference value 'N' to determine the difference therebetween, and output the result to the clock generator 206 in a later stage", col. 7 lines 16-19).

Claim 24, *the packet pre-processor* ("pre-processor" of fig. 6 as discussed above for claim 23) *comprises:*

a pre-compute circuitry (fig. 7 "counter 501" and "latch section 502") *to calculate a total bit group of data received* ("count n" cited above and shown in fig. 7 as output from said "latch section 502", for which see "The latch section 502 latches the count n counted by the counter 501", col. 7 lines 5-6) *by the packet pre-processor at the input data rate* (see "The count n represents a value corresponding to the average input rate in a given period", col. 7 lines 33-34); *and*

a request modifier circuitry (fig. 7, "comparator 504" and "clock generator 206") *coupled to the pre-compute circuitry* (fig. 7 depicting such coupling), *the request modifier circuitry to determine a difference between the total big group of*

data calculated by the pre-compute circuitry (fig. 7 depicting "count n" as an input to said "comparator 504") *and a predetermined output data bus width* (fig. 7 "reference value (N)", and see further "The comparator 504 compares the count n latched by the latch section 502 and the reference value 'N' to determine the difference therebetween, and output the result to the clock generator 206 in a later stage", col. 7 lines 16-19).

Minoda does not expressly disclose, regarding claim 5, *generating additional read requests*; regarding claim 6, *masking data read requests*; and regarding claim 11, *performing at least one of masking a data read request and generating an additional data read request* (see "The speed correction amount calculator 303 matches the difference between the average input rate [n] and the reference output rate [N]", col. 8 lines 22-24).

However, Costello discloses:

Regarding claim 5, for "**B**ehind case", *generating additional read request*.

Regarding claim 11, *performing generating an additional data read request.*

(see discussion above regarding claim 1, i.e., Costello disclosing "initiates additional read operations")

Burk discloses:

Regarding claim 6, for "**A**head of case", *masking read requests.*

Regarding claim 11, *performing masking a data read request.*

(see discussion above regarding claim 1, i.e., Burk disclosing "inhibit performance of the read transaction initiated by the read request (e.g., by buffering the read request and delaying to provide the read request)").

3. Claims 4 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Minoda in view of Burk and Costello, as applied to claims 1 and 20, and further in view of Norizuki et at (US 5,357,510, Norizuki hereinafter).

Minoda in view of Burk and Costello discloses claimed limitations as discussed in section 2, including that *the variation is compensated.*

Minoda in view of Burk and Costello does not disclose, regarding claim 4, [the variation is compensated] *to decrease a number of idle cell insertions;* regarding claim 21, *wherein the means for compensating decreases a number of idle cell insertions.*

Norizuki discloses “an apparatus for supervising and controlling ATM traffic” (Abstract lines 1-2) having a "control unit for performing the operation of traffic control in accordance with the idle cell rate provided” (Abstract lines 15-16) comprising for

Regarding claim 4, [the variation is compensated] *to decrease a number of idle cell insertions;*

Regarding claim 21, *means for decreasing a number of idle cell insertions.*

(refer to figs. 6 and 7 and see “fig. 7 shows an example of a variation of the ratio of idle cells to user information cells on a transmission line … and a total band width consists of an idle cell band width and a user band width", col. 6 lines 31-36, noting that fig. 7 shows in some cases idle cells are inserted *to a decreased number* than some other cases).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the method/apparatus of Minoda by adding the idle cell insertion

feature of Norizuki to Minoda in order to provide more instantaneously responsive system "for traffic supervisory control that ordinarily monitors the band capacity of a transmission line … to also be able to cope with burst conditions of the traffic fluctuation" (Norizuli, col. 3 lines 41-47).

4. Claims 9, 13, 14, 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Minoda in view of Burk and Costello, as applied to claims 1 and 15 above, and further in view of Modelski et at (US 2002/0120798, Modelski hereinafter).

Minoda in view of Burk and Costello discloses claimed limitations discussed in section 2 above. Minoda further discloses:

Regarding claim 9, *transmitting an output data stream to an output* buffer (fig. 6 "ring buffer memory 201");

passing the data read requests to an input buffer (fig. 6 "ring buffer memory 201", and see "The read address generator 204 is a circuit for generating the address of output data according to clocks generated by the clock generator 206", col. 6 lines 50-52, which effectively *passes read requests* as well known in the art) *when the output* buffer *is not substantially full* (this is well known in the art as well as intuitive also).

Regarding claim 13, *passing the data read request to an input* buffer (fig. 6 "ring buffer memory 201", and see "The read address generator 204 is a circuit for generating the address of output data according to clocks generated by the clock

generator 206", col. 6 lines 50-52, which effectively *passes read requests* as well known in the art).

Regarding claim 14, *passing the data read request and the additional data read request to an input* buffer (fig. 6 "ring buffer memory 201", and see, for *the data read request*, "The read address generator 204 is a circuit for generating the address of output data according to clocks generated by the clock generator 206", col. 6 lines 50-52, which effectively *passes read requests* as well known in the art; and see further, for *the additional data read request* , e.g., "When the relation between the count n and the reference value N is n < (0.98×N), the count n is judged to be (-2%), i.e., 2% behind the reference value N", col. 7 lines 41-43, and then "The speed correction amount calculator 303 matches the difference between the average input rate [n] and the reference output rate [N]", col. 8 lines 22-24, which inevitably results in *additional read request*).

Regarding claim 17, *a link layer device* (fig. 6 "write address generator 202");

an input buffer (fig. 6 "ring buffer memory 201") *coupled to the request modifier circuitry* (fig. 7, "comparator 504" and "clock generator 206"), *link layer device* (fig. 6 "write address generator 202") *and the pre-compute circuitry* (fig. 7 "counter 501" and "latch section 502", and fig. 6 depicting such coupling), *the input* buffer *to receive input data at the input data rate* (fig. 6 depicting "ring buffer memory 201" receiving "data after sampling rate conversion"); *and*

an output buffer (fig. 6 "ring buffer memory 201") *coupled to the encapsulator engine and the request modifier circuitry* (fig. 6 depicting said coupling), *the output* buffer *to transmit output data* (fig. 6 "DA data") *at the predetermined output data rate*

(see “correcting the difference between the average input rate and the reference output rate”, col. 8 lines 14-15).

Regarding claim 18, *a frame engine* (fig. 6 “parallel/serial converter 207”) *coupled to the output* buffer (fig. 6 “ring buffer memory”); *and*

a physical interface (fig. 1 “output interface 8”) *device coupled to the frame engine* (noting that said "parallel/serial converter” as part of the “digital data buffering device” shown in fig. 6 “is applied to the output interface 8 [of fig. 1]", col. 6 line 24)

Regarding claim 19, *the pre-compute circuitry receives input data from the input* buffer, *the encapsulator engine receives the input data from the pre-compute circuitry, the output* buffer *receives the output data from the encapsulator engine, the request modifier circuitry receives data read requests from the frame engine, the link layer device receives the data read request from the request modifier circuitry* (figs. 6, 7 and 9 in combination depicting such data flow steps, noting the fact that Minoda's "ring buffer memory” plays a dual role of input/output buffers).

Minoda does not disclose, regarding claims 9, 13, 14, 17-19, said input/output buffers are of *first-in-first-out (FIFO)*; and regarding claim 9, *determining when the output FIFO is substantially full* and *masking the data read request to the input FIFO when the output FIFO is substantially full.*

Modelski discloses a “Global access bus architecture includes a master request bus and a slave request bus separated from each other and pipelined” (Abstract lines 1-2) wherein “pipelines operate on the read request" ([0203] lines 5) comprising the above cited features missing from Minoda, particularly:

Regarding claims 9, 13, 14, 17-19, using separate input/output *FIFOs* (see "input and output FIFOs buffer");

Regarding claim 9, *determining when the output FIFO is substantially full; and masking the data read request to the input FIFO when the output FIFO is substantially full* (see "The input and output FIFOs buffer data flow between the pipelines and the MUXs. Since lookups and filters can be forwarded from one [memory] bank to the other (depending on the contents of the back forwarding registers), a lockout condition can occur where the output FIFOs for each bank are full and each input FIFO has a lookup that needs to continue … This is controlled by the MUXs that do not allow more than 32 operations to be submitted across both pipelines", [0204] lines 1-9).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the method of Minoda by adding Modelski's input/output FIFO and lookup lockout mechanism upon detecting a full output FIFO being in order to provide a more robust method/device which further "provides fast path processing and enhanced flexibility/adaptability of packet processors" (Modelski, [0013] lines 4-5).

5. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Minoda in view of Burk, Costello and Modelski, as applied to claim 9 above, and further in view of Rajaraman (US 5,802,310).

Minoda in view of Burk, Costello and Modelski discloses claimed limitations discussed in section 4 above including Modelski disclosing using output FIFO and

determining the fullness of the FIFO. Minoda in view of Burk, Costello and Modelski however does not disclose *substantial full is a set value determined by a value representative of an amount of data contained in a number of stages of a pipeline subtracted from another value representative of a capacity of the output FIFO*.

Rajaraman discloses "systems and methods for data channel queue control in a communications network" (col. 1 lines 1-3) wherein, refer to fig. 5, "data transfer controlling 54" to "queue 56" is based on "queue limit determining 58". Rajaraman's methods further comprises *substantial full is a set value determined by a value representative of an amount of data contained in a number of stages of a pipeline subtracted from another value representative of a capacity of the output FIFO* (see firstly, "more commonly, a 'high-water mark" (HWM) less than the queue capacity and a 'low-water mark' (LWM) greater than empty are established for the data store", col. 3 lines 30-33, and secondly, Rajaraman provides further improvements, see fig. 6, step 71 "is amount of queued data greater than first limit [corresponding to HWM]?" and, if the answer is "Yes", step 71a "disable data transfer from application to queue").

It would have been obvious to one of ordinary skill in the art at the time of the invention to further modify the method of Minoda by adding the queue limit mechanism of Rajaraman in order to provide a more efficient system "which dynamically optimize queue parameters such as high water mark (HWM) and low water mark (LWM) in response to network and node conditions" (Rajaraman, col. 4 lines 6-8).

6. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Minoda in view of Burk and Costello, as applied to claim 20 above, and further in view of Kuo et at (US 6,047,001, Kuo hereinafter).

Minoda in view of Burk and Costello discloses claimed limitation in section 2 above except *compensating for invalid bytes of an input data stream.*

Kuo discloses "a network interface device having a random access memory for buffering data" (Abstract lines 1-2) using a "frame information generation" unit (fig. 4 item 82) comprising:

Regarding claim 22, *compensating for invalid bytes of an input data stream* (see, in reference to figs. 4 and 5, "the frame information generation logic 82 determines the count value (CNT) by subtracting the value of the write pointer 90, minus the address value in the start address 92, minus the invalid byte count determined from the byte enable value (BE-L) in step 106a", col. 10 line 67 – col. 11 line 5).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the method of Minoda by adding the invalid data subtraction mechanism of Kuo to Midona in order to provide a more efficient system "enabling a read controller to quickly determine the status of a stored data frame by accessing the corresponding tracking information" (Kuo col. 3 lines 9-11).

7. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Minoda in view of Burk and Costello, as applied to claim 23 above, and further in view of Zelikovitz et at (US 5,555,478, Zelikovitz hereinafter).

Minoda in view of Burk and Costello discloses claimed limitations in section 2 above. Minoda further discloses:

Regarding claim 25, *a second physical interface device* (fig. 1 “output interface 8”) *coupled to the link layer device* (said “link portion” discussed for claim 23 above), *wherein the second physical interface device, the link layer device, the framer* (fig. 6 “digital data buffering device”) *and the first physical interface device* (fig. 1 “input interface”) *reside in a* data processor (fig. 1 “a sampling rate converter" showing all said elements).

Minoda in view of Burk and Costello does not expressly disclose that said data processor (“sampling rate converter”) is *a line card.*

Zelikovitz discloses a "fiber optic information transmission system” (col. 2 lines 1-2) having a “thirty two (32) subscribers linked to four (4) fiber optic cables in the fiber optic network” (fig. 2A and col. 2 lines 1-3) comprising the above feature, i.e., using *line card* as a data processor (refer to fig. 2A item 120 and see “This line card 120 is a data processor capable of manipulating data appropriately to form the transmission packet”, col. 9 lines 24-25).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the device of Minoda by adding the line card feature of Zelikovitz to Minoda in order to provide a scalable system that “establishes a digital information network having a very high capacity" (Zelikovitz, col. 1 lines 57-58)

8. Claims 26 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Minoda in view of Burk, Costello and Zelikovitz, as applied above to claim 25, and further in view of Duplessis et at (US 2002/0,191,617, Duplessis hereinafter).

Minoda in view of Burk, Costello and Zelikovitz discloses claimed limitations in paragraph section 8 above except regarding claim 26, *wherein the second physical interface device is an Ethernet device and the first physical interface device is a Synchronous Optical Network (SONET) device;* regarding claim 27, *wherein the line card is coupled to a wide area network (WAN).*

Duplessis discloses a "system and method for transporting channelized Ethernet over SONET/SDH" (page 1 left col. lines 1-2) using, referring to fig. 3, "a preferred network element 12 that is capable of allowing communication path between network systems Net1 and Net2" ([0020] lines 1-3, which Net1 and Net2 are shown in fig. 2) comprising the above cited features, particularly:

Regarding claim 26, *wherein the second physical interface device is an Ethernet device and the first physical interface device is a Synchronous Optical Network (SONET) device* (refer to figs. 3 and 4 and see "the mapper module 14 in the preferred network element 12 maps a traffic port such as an Ethernet port onto the STS-48c", [0021] lines 8-10, which "STS-48c" is a well-known SONET data standard, which is also depicted in fig. 3 by "SONET/SDH" output from "line card 18").

Regarding claim 27, *wherein the line card is coupled to a wide area network (WAN)* (refer to fig. 2 and see "the network systems Net1, Net2, Net3, and Net4

could be local area networks (LANs), metro area networks (MANs), wide area networks (WANs)", [0019] last four lines).

It would have been obvious to one of ordinary skill in the art at the time of the invention to further modify the method/device of Minoda by adding the SONET/Ethernet/WAN feature of Duplessis to Minoda in order to provide a more flexible and efficient method/system that is able "to map a payload size of y into x when y<<x" (Duplessis, [0005] lines 7-8).

Allowable Subject Matter

9. Claims 7 and 29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 7/29 provide detailed steps of controlling *data read request* of which the following features/steps appear to be allowable subject matter:

subtracting the difference from the counter value…
masking a data read quest transmitted from a packet encapsulator to the input FIFO when the counter value is either equal to or less/greater than the lower/upper threshold value, wherein the lower/upper threshold value is the negative/positive value of the pre-determined output data bus width; and
generating an additional data read request to be transmitted from the packet encapsulator to the input FIFO when the counter value is either equal to or greater/less than the upper/lower threshold value, wherein the upper/lower threshold value is the positive/negative value of the pre-determined output data bus width.

It is noted that the closest prior arts of Minoda and Modelski, singularly or in combination fail to anticipate the above underlined features or render them obvious.

(**Examiner's note**: It is noted hereby that the nominal difference for claims 7/29 reflected in *lower/upper* threshold values being *negative/positive* of the *pre-determined output data bus width* comes from the difference in defining the *counter value*, which is *representative of the variation* between the *input data rate* and the *output data rate*, as set forth in claims 1/28 that 7/29 depend from, respectively. In the case of claim 7, the *counter value* is (output rate − input rate), while in the case of claim 29, it is (input rate − output rate). It is further noted herein that either definition provides no advantages or disadvantages over the other)

Response to Arguments

10. Applicant's arguments with respect to claims 1, 15, 20 and 23 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's arguments are against previously applied art of Minoda over the newly added features of *masking read requests* and/or *generating additional read requests* under two different *threshold conditions.* Said newly added features are taught by Burk on *masking read requests* and Costello on *generating additional read requests*, and thus the arguments are moot.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ANDREW LAI whose telephone number is (571)272-9741. The examiner can normally be reached on M-F 7:30-5:00 EST, Off alternative Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kwang Yao can be reached on 571-272-3182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Andrew Lai/
Examiner, Art Unit 2616

/Kwang B. Yao/
Supervisory Patent Examiner, Art Unit 2616